REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed Dec. 17, 2003. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

1.Present Status of the Application

Upon entry of the amendments in this response, claims 61-94, and 102-134 remain pending in the present application. More specifically, claims 61, 64-67, 69, 70, 72-94, 102 and 105-134 are directly amended; and claims 95-101, and 135-138 are canceled without prejudice, waiver, or disclaimer. These amendments are specifically described above. It is believed that the foregoing amendments add no new matter to the present application.

2.Response To Objections/Rejections

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response To Claim Rejections Under 35 U.S.C. Section 102

As originally recited, independent claim 61 recites below:

61. A chip packaging method comprising:
providing a bulk metal substrate without conductive traces;
providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface;
mounting the dies onto the bulk metal substrate, the backside of the dies facing the bulk metal substrate; and
forming a plurality of patterned lines over the active surface of the dies, ***wherein the patterned lines are constructed from at least a patterned wiring layer.***

(emphasis added)

Yamazaki discloses that multiple CMOS circuits and pixel matrix circuits are directly formed on a metal substrate 100. However, the present invention discloses that dies where active devices have been formed are mounted on a bulk metal substrate, which is not taught by Yamazaki. The withdrawal of the rejection is respectfully reconsidered for at least the reason that Yamazaki al. fails to disclose or suggest the features that are highlighted in claim 61 above.

As currently amended, independent claim 102 recites below:

102. A chip packaging method comprising:
providing a first substrate;
providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface;
mounting the dies over the first substrate, the active surfaces of the dies facing the first substrate;
thinning the dies from their backsides;
providing a second substrate;
mounting the second substrate over the backsides of the dies;
removing the first substrate; and
forming a plurality of patterned lines over the active surface of the dies.

(emphasis added)

The withdrawal of the rejection is respectfully reconsidered for at least the reason that Yamazaki al. fails to disclose or suggest the features that are highlighted in claim 102 above.

Response To Claim Rejections Under 35 U.S.C. Section 103

As originally recited, independent claim 61 recites below:

61. A chip packaging method comprising:

providing a bulk metal substrate without conductive traces;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface;

mounting the dies onto the bulk metal substrate, the backside of the dies facing the bulk metal substrate; and

forming a plurality of patterned lines over the active surface of the dies, ***wherein the patterned lines are constructed from at least a patterned wiring layer***.

(emphasis added)

Applicant respectfully asserts that the chip packaging method claimed in claim 61 patentably distinguishes over Yamazaki's method and Wojnarowski's method.

Yamazaki discloses that *multiple CMOS circuits and pixel matrix circuits are directly formed on a metal substrate 100*. However, the present invention discloses that *dies where active devices have been formed are mounted on a bulk metal substrate*. Moreover, Wojnarowski fails to disclose that multiple dies can be mounted on a *bulk metal substrate*. It is should be noted that the technology field that active devices are directly formed on a substrate is significantly different from the technology field that dies where active devices have been formed are mounted on a substrate. Therefore, the reference by Yamazaki teaches away from that by Wojnarowski, so applicants consider Yamazaki's method can not be combined with Wojnarowski's method. Withdrawal of these rejections is respectfully requested.

Applicant respectfully asserts that the chip packaging method claimed in claim 61 patentably distinguishes over Cole's method, Mowatt's method and Dove's method.

Cole discloses that multiple dies 12 can be mounted on a substrate 11. However, *Cole fails to teach, hint or suggest that the substrate 11 is a bulk metal substrate*. Mowatt discloses

that the substrate for carrying dies comprises multiple patterned metal layers and multiple laminate layers. *Mowatt fails to disclose that dies can be mounted on a bulk metal substrate without conductive traces*. Dove discloses that conductive wires 155 formed by a wire-bonding process are connected to a die 110. However, *Dove fails to teach, hint or suggest that there is a patterned wiring layer formed over the dies by electroplating and sputtering processes, for example. The conductive wire 155 is not shaped like a layer, and, therefore, the patterned wiring layer*, recited in claim 61, *is distinct from the conductive wire 155 formed by a wire-bonding process*, taught by Dove. It is should be noted that the technology field that patterned lines are formed by a wire-bonding process is significantly different from the technology field that the patterned lines are constructed from one or more patterned wiring layers. Therefore, the reference by Dove teaches away from that by Cole and that by Mowatt, so applicants consider Cole's method and Mowatt method can not be combined with Dove's method. Therefore, withdrawal of these rejections is respectfully requested.

As originally recited, independent claim 102 recites below:

102. A chip packaging method comprising:
providing a first substrate;
providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface;
mounting the dies over the first substrate, the active surfaces of the dies facing the first substrate;
thinning the dies from their backsides;
providing a second substrate;
mounting the second substrate over the backsides of the dies;
removing the first substrate; and
forming a plurality of patterned lines over the active surface of the dies.

(emphasis added)

Applicant respectfully asserts that the chip packaging method claimed in claim 102 patentably distinguishes over Yamazaki's method and Wojnarowski's method.

Yamazaki discloses that *multiple CMOS circuits and pixel matrix circuits are directly formed on a substrate 100*. However, the present invention discloses that *dies where active devices have been formed are mounted on a substrate*. Moreover, Wojnarowski fails to disclose that multiple dies are mounted on a first substrate, wherein *the active surfaces of the dies face the first substrate*. It is should be noted that the technology field that active devices are directly formed on a substrate is significantly different from the technology field that dies where active devices have been formed are mounted on a substrate. Therefore, the reference by Yamazaki teaches away from that by Wojnarowski, so applicants consider Yamazaki's method can not be combined with Wojnarowski's method. Therefore, withdrawal of these rejections is respectfully requested.

Moreover, *Yamazaki and Wojnarowski fail to disclose, hint or suggest a thinning process can be performed*.

Applicant respectfully asserts that the chip packaging method claimed in claim 102 patentably distinguishes over Cple's method, Mowatt's method and Dove's method.

Cole, Mowatt and Dove disclose that multiple dies are mounted on a substrate, wherein the backsides of the dies face the substrate. However, *Cole, Mowatt and Dove fail to teach, hint or suggest that the active surfaces of the dies face a substrate*. Moreover, *Cole Mowatt and Dove fail to teach, hint or suggest that a thinning process is performed*. All of the citations by

Cole Mowatt and Dove do not disclose the characteristics in claim 102, so withdrawal of these rejections is respectfully requested.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 61 and 102 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 62-94, and 103-134 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 61-94, and 102-134 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date: 3/17/2004

Jiawei Huang
Registration No. 43,330

J.C. Patents
4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax : (949) 660-0809